**DAILY ASSESSMENT FORMAT**

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| **Date:** | **2 June 2020** | **Name:** | **Shreya poojary** |
| **Course:** | **HDL design** | **USN:** | **4al16ec074** |
| **Topic:** | **Analysis of clocked sequential circuits**  **Digital clock design** | **Semester & Section:** | **8-B** |
| **Github Repository:** | **Shreya-test** |  |  |

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| **Image of session** |
| **Report**    **The main parts of the circuit are as follows:**   1. **Timer 555**:   Responsible for generating the clock pulses for the counters, the frequency of the output shoul be 1 hz which means 1 second for each pulse.   1. **Counters**:   Responsible for generating the time in BCD (Binary Coded decimal).   1. **Decoders**:   Takes the BCD of the counter as input and produces 7 segment output .  **The circuit works as follows :**  555 timer produces 1 seconde pulses to the clock input of the first counter which is responsible the first column of seconds, so its output will change every second.  The counter produces numbers from 0 to 9 in BCD form and automatically resets to 0 after that.  so the output of the first counter will count from 0 to 9 every second and that's exactly what we want from it, so we are done here. let's move to the next one. **The JK Flip Flop:** The JK Flip-flop is similar to the SR Flip-flop but there is no change in state when the J and K inputs are both LOW  The basic S-R NAND flip-flop circuit has many advantages and uses in sequential logic circuits but it suffers from two basic switching problems.   * 1. the Set = 0 and Reset = 0 condition (S = R = 0) must always be avoided * 2. if Set or Reset change state while the enable (EN) input is high the correct latching action may not occur   Then to overcome these two fundamental design problems with the SR flip-flop design, the **JK flip Flop** was developed.  This simple **JK flip Flop** is the most widely used of all the flip-flop designs and is considered to be a universal flip-flop circuit. The two inputs labelled “J” and “K” are not shortened abbreviated letters of other words, such as “S” for Set and “R” for Reset, but are themselves autonomous letters chosen by its inventor Jack Kilby to distinguish the flip-flop design from other types.  The sequential operation of the JK flip flop is exactly the same as for the previous SR flip-flop with the same “Set” and “Reset” inputs. The difference this time is that the “JK flip flop” has no invalid or forbidden input states of the SR Latch even when S and R are both at logic “1”.  The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”. The symbol for a JK flip flop is similar to that of an *SR Bistable Latch* as seen in the previous tutorial except for the addition of a clock input. |